Guidance for students who take Hardware Design I
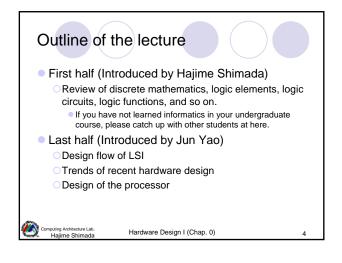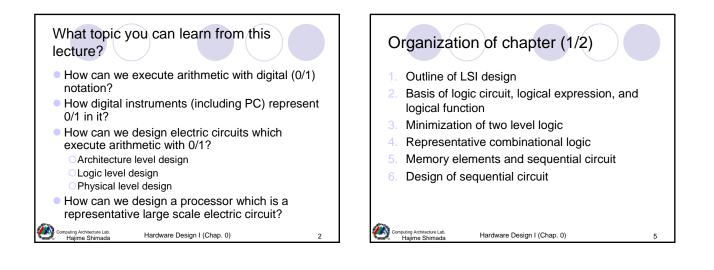
Computing Architecture Lab.

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What topic you can learn from this lecture?

- How can we execute arithmetic with digital (0/1) notation?
- How digital instruments (including PC) represent 0/1 in it?
- How can we design electric circuits which execute arithmetic with 0/1?
  - Architecture level design
  - Logic level design
  - Physical level design
- How can we design a processor which is a representative large scale electric circuit?

What enable you after you finished Hardware Design I?

- For hardware related researches
  - You can get a basic knowledge about hardware design
- For software related researches
  - You may image hardware (processor) organization when you optimize program
  - You may promote your research with specific designed hardware accelerator
    - e.g. GRAPE: a special purpose computer system for astrophysical many-body simulations
    - Recent improvement on programmable hardware gives much advantage about this area

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Outline of the lecture

- First half (Introduced by Hajime Shimada)
  - Review of discrete mathematics, logic elements, logic circuits, logic functions, and so on.
    - If you have not learned informatics in your undergraduate course, please catch up with other students at here.
- Last half (Introduced by Jun Yao)
  - Design flow of LSI
  - Trends of recent hardware design
  - Design of the processor

Organization of chapter (1/2)

1. Outline of LSI design
2. Basis of logic circuit, logical expression, and logical function
3. Minimization of two level logic
4. Representative combinational logic
5. Memory elements and sequential circuit
6. Design of sequential circuit

Organization of chapter (2/2)

7. Optimization of two level circuit and synthesis of multi level circuit
8. Simplify of multi level circuit
9. Technology mapping, place, and route
10. Programmable hardwares
11. Design of microprocessor
12. Latest processors and hardware design topics

Note that this plan will be changed depending on your understanding

Schedule

- 1: Dec. 1 (Thu)
- 2: Dec. 5 (Mon)
- 3: Dec. 8 (Thu)
- 4: Dec. 12 (Mon)
- 5: Dec. 15 (Thu)
- 6: Dec. 19 (Mon)
- 7: Dec. 22 (Thu)
- Holiday: Dec. 26 (Mon)
- Holiday: Dec. 29 (Thu)
- Holiday: Jan. 2 (Mon)
- Holiday: Jan 5 (Thu)
- Holiday: Jan 9 (Mon)
- 8: Jan 12 (Thu)
- 9: Jan 16 (Mon)
- 10: Jan 19 (Thu)
- 11: Jan 23 (Mon)
- 12: Jan 26 (Thu)
- 13: Jan 30 (Mon)
- 14: Feb. 2 (Thu)
- 15: Feb. 6 (Mon)
  - Term end examination

Grading

- Small examination (40%)
  - Randomly done in the lecture
    - Around 8 times
  - Around 10 minutes length
  - If you felt that you failed the answer, please submit revised answer as a report
- Term end examination (60%)
  - On Feb. 6 (Mon)
  - 90 minutes length
  - Range of topic will be announced in the class and web

The rule of the examinations

- You can see handout of lecture and your notebook
  - You can see PDF version of handout on your PC, but you must not use search function
    - At least, you have to create index of topics in your brain
- If you absent examinations with legal reason, you can take supplemental exam
  - e.g. disease, presentation in academic conference
  - Please submit the document which proofs the legality

How to get handout

- Please get handout with yourself from next time
- URL: http://arch.naist.jp/~shimada/HW_design/index.html
  - Can not access from outer NAIST
  - I'll place it until 12:00 of preceding day

How to contact to Shimada or Yao

- Come to B403 (Shimada) or B405 (Yao) room
  - If I'm free, I'll keep door with open state
  - Usually, I'm here from 10 a.m. to 9 p.m.
  - Current our status (e.g. on business trip) is denoted on our door
- Send e-mail to shimada@is.naist.jp or yaojun@is.naist.jp
- Call 5301(Shimada)/5302(Yao) in internal phone line or 0743-72-5301/5302 on the phone