Hardware Design I Chap. 1
Outline of LSI Design

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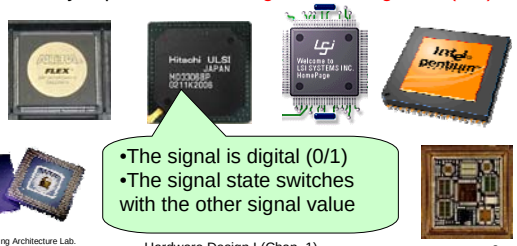
Outline of Chap. 1

- Definition of digital system
- History of digital system
  - From vacuum bulb to field effective transistor (FET)
- The physical image of current device
  - Metal Oxide Semiconductor (MOS) FET
  - CMOS organization (CMOS NAND, CMOS NOR)
- Outlined flow of LSI design
- Outlined flow of semiconductor process

What is a digital system?

- The system which process information with digital notations
  - Usually implemented as Large Scale Integration (LSI)



•The signal is digital (0/1)
•The signal state switches with the other signal value

What is digital notation?

- It only allows two values: 0 or 1
  - Discrete values -> manipulated under discrete mathematics rules (logical operation) -> Chap. 2
  - Easy to allocate ON or OFF status in electric circuits
- Suitable to current field effective transistor based electric circuits -> later Chap. 1
  - We can also implement same function with analog circuit, but it requires further costs
  - Analog value in practical world is translated via analog-digital converter (AD converter)
    - Also there's DA converter to translate processed result

How to represent 0/1 in electric circuits

- We have to define representation on electric circuit
- In usual circuit, we use high/low voltage
  - 0: low voltage (conducted to ground)
  - 1: high voltage (conducted to power supply)
- The other representations
  - Current (relay)
  - Spin of electron (spintronics)
  - Single quantum flux (superconductive element)

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Relay: a primitive switch

- It can control current ON/OFF status by the other current
  - Utilize electromagnet to control output current
  - Represent 0/1 with current
    - 0: current does not flow
    - 1: current flows

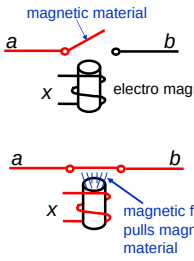
Exterior of relay

Inputs of control signal (*x* in next slide)

Outputs of relay (*a* and *b* in next slide)

Operation of the relay

- Open or close switch with the current supplied to electro magnet



a and *b* are not conducted if *x* = 0 (without current)

a and *b* are conducted if *x* = 1 (with current)

Sample basic logic operation

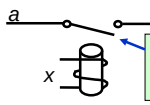
- Let's achieve these operation with relay
  - Logical product (AND)
    - Output becomes 1 if both of two input is 1
    - Otherwise output is 0
  - Logical addition (OR)
    - Output becomes 1 if either of two input is 1
    - Otherwise output is 0
  - Negation (NOT)
    - Output becomes 0 if input is 1
    - Output becomes 1 if input is 0

Detail of logic operation -> Chap. 2 and 3

Logical function with relay (1/2)

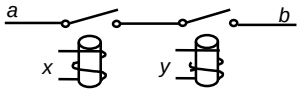
- We can represent logic function by relay

NOT function: $\overline{x}$ or x'



a and *b* are conducted if *x* = 0 and not conducted if x = 1 (inverse action)

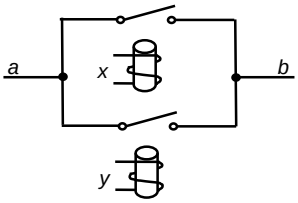
AND function: $x \cdot y$



Logical function with relay (2/2)

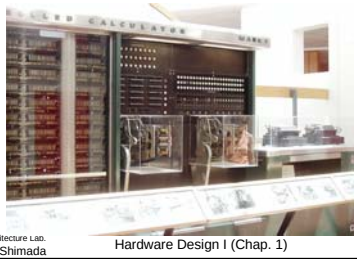
- We can represent logic function by relay

OR function: $x + y$



Computer constructed with relay

- Harvard Mark I (1944)
  - Utilizes about 3,300 relays
  - Operate multiply in 5.7 sec. and division in 15.3 sec.



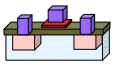
Transition of switch

Relay

- Mechanical abrasion makes it broken
- Operation speed limit from physical behavior

Vacuum bulb

- Breaks as well as lamp bulb
- Used around 1940s to 1950s



Transistor

- Hard to break
- Still integrated even in latest ULSI
- Used after 1950s

Quiz

- What is the first computer in the world (using vacuum bulb)?
  1. ENIVAC
  2. ENIAC
  3. EDSAC
  4. EDVAC
- Note that there's some "the first computer" candidates, but please choose most famous one

Answer

- 2. "ENIAC"
  - Other candidates: Atanasoff-Berry Computer, Zuse Z3
- 3. "EDSAC" is also famous as a the first "neuman type computer"
  - Other candidates: Manchester SSEM

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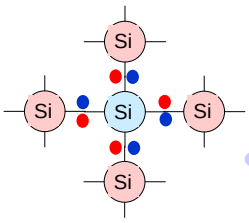
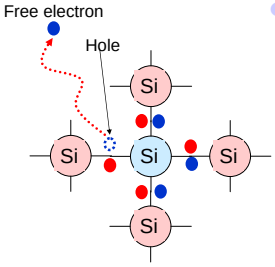
Semiconductor

Si (silicon) has
4 valence electrons



- Half conduct the electric current
  - Usually, there's no free electron
  - By adding voltage (over threshold), the electron can move
- If we dope some impurity, the conductivity increases dramatically

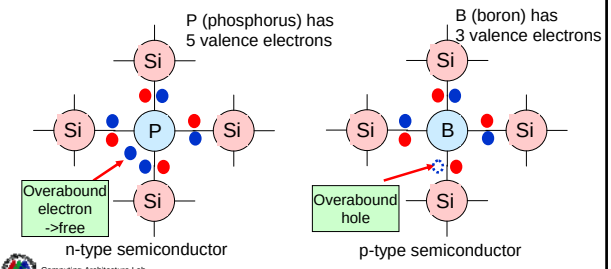
Hole and free electron



- Voltage load sometimes moves electron and creates hole and free electron
  - Hole: A space which electron has existed
  - Free electron: A electron which can move freely

Impurity semiconductor

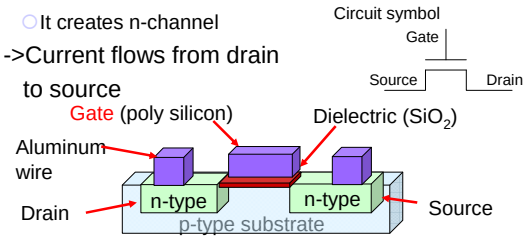
- Doped impurity creates overabound electron or hole
- Additional electron or hole carries current



nMOS field effect transistor (FET)

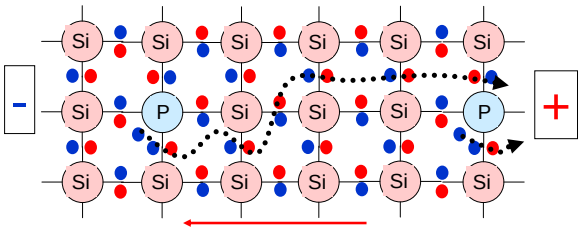
- If we add voltage to gate, electrons gather under dielectric
  - It creates n-channel

->Current flows from drain to source



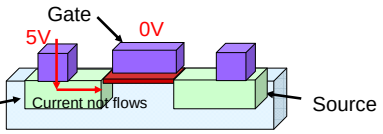
Current flow of n-type semiconductor

- The movement of free electrons create current

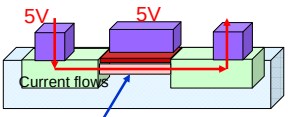


Operation of nMOS FET

- OFF state



- On state

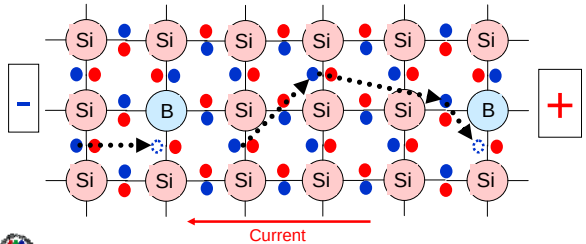


n-channel (flood with electron) has created

Current flow of p-type semiconductor

- The movement of hole create current
  - The fixed electron moves and trapped at hole

->The hole moves to the point where the electron has existed

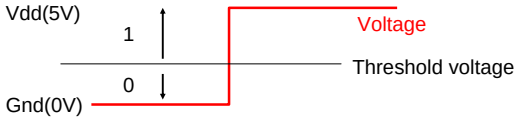


Why it called MOS transistor?

- Metal
  - Aluminum (traditional), copper (current)
- Oxide
  - SiO_2 (traditional), HfON (current high-end)
- Semiconductor
  - Silicon
  - In the future: carbon nano tube???

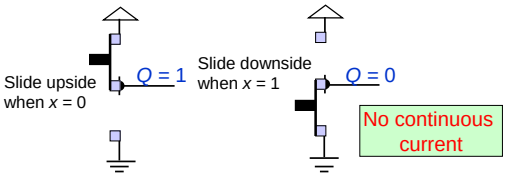
Digital (0/1) notation with FET

- 0 state is denoted with the voltage of ground (0V)
- 1 state is denoted with the voltage of supply voltage (5V, 3.3V, 2.5V, 1.8V, 1.5V, and so on)
  - Denoted as Vcc or Vdd
  - Vdd differs in semiconductor process technology



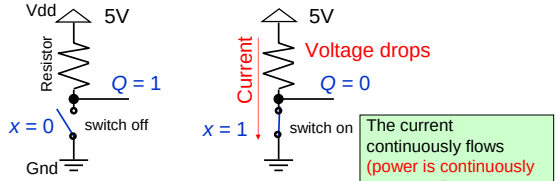
NOT logic with slide switch

- Let assume slide switch
- It does not consume energy in steady state
- Next step: let's create slide switch with MOS



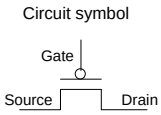
Creating NOT logic with switch

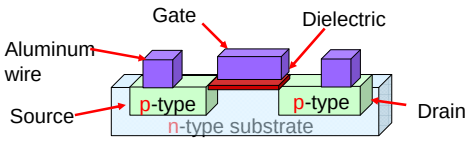
- NOT logic
  - Assuming 1 input *x* and 1 output *Q*
  - *Q* = *x'* (negative value of *x*)
- Let's create it with switch



pMOS field effect transistor (FET)

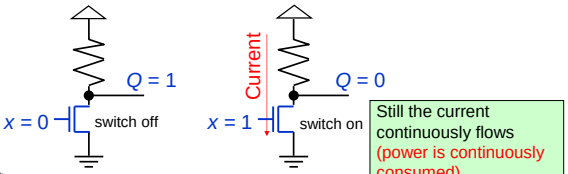
- pMOS FET which has opposite characteristic to nMOS FET
- If we add voltage to gate, holes under dielectric banish





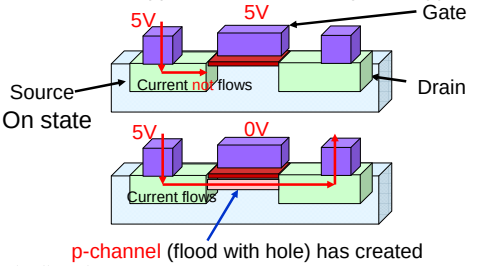
Creating NOT logic with nMOS FET

- We can replace switch to nMOS FET
  - This is an ancient implementation to save number of FET
- Problem of this organization
  - Consumes huge power
  - Next step: let's eliminate continuous current



Operation of pMOS FET

- OFF state
  - Channel disappears when the voltage has applied



- On state

nMOS and pMOS

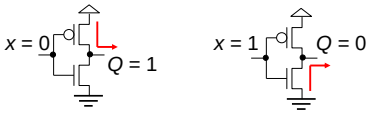
nMOS FET
- OFF state if input is 0
- ON state if input is 1
- The career is electron

pMOS FET
- OFF state if input is 1
- ON state if input is 0
- The carrier is hole
  - Maximum current is half of that of nMOS

We can prepare complementally switch

CMOS NOT logic

- CMOS: Complementary MOS
  - Combines nMOS and pMOS
- Does not consume energy in steady state



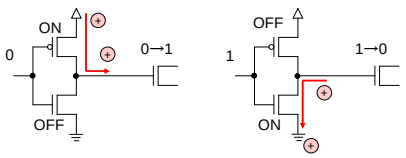
Upside is ON, downside is OFF

Upside is OFF, downside is ON

Basic of power consumption on CMOS logic

- In CMOS circuit, charge moves to Gnd with following procedure
  - Charge moves to Vdd to output node with input 0
  - Charge moves to output node to Gnd with input 1

0 -> 1 -> 0 transition makes one unit of power consumption



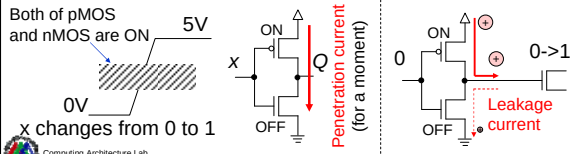
Equation of CMOS power consumption

$$\text{Power} \propto C \times F \times V^2$$

- C: Capacitance
  - Capacitance of output node
  - Internal FET capacitance
- F: Frequency
  - Clock frequency in synchronous circuit
  - Otherwise, number of switching
- V: Supply voltage

Power consumption in CMOS NOT logic (Advancement)

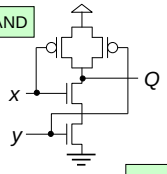
- Penetration current under transition
  - Both pMOS and nMOS conducts for a moment
- Leakage current
  - Few current flows even in OFF state
  - Let assume the faucet which cannot fully close and leaks water



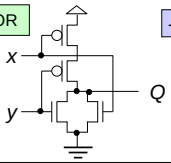
CMOS NAND and NOR

- 2 input NAND (NOT AND)
  - $Q = 0$ if both x and y is 1, otherwise $Q = 1$
- 2 input NOR (NOT OR)
  - $Q = 1$ if both x and y is 0, otherwise $Q = 0$

NAND



NOR

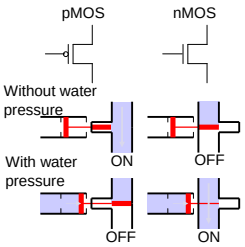


-> Chap. 2

We can create logic gate by combining FET

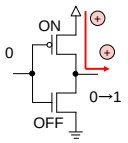
Water pressure logic

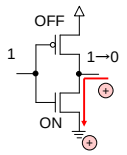
- Let's create logic in some other material
- e.g. water pressure logic
  - Create pMOS and nMOS like water valve
  - They operate with input side water pressure



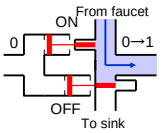
Water pressure NOT logic

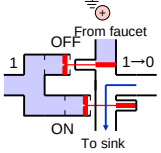
- Combining valve to create NOT logic
  - Vdd = faucet
  - Gnd = sink
  - Current = water flow





If we create some operateable logic with it, I think that it becomes good art work





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About integrated circuits (1/2)

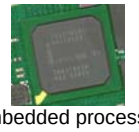
- Semiconductor technology allows integrating many transistors into one silicon chip
- Level of integration
  - Integrated circuit (IC): less than 1000 transistors
  - Large scale integration (LSI): thousands to 10 thousands transistors

Logic IC TTL7400 (8 Tr)

Microcontroller STM32F103 (33,000 Tr)

About integrated circuits (2/2)

- Level of integration
  - Very Large scale integration (VLSI): more than 100 thousand transistors
  - Ultra Large scale integration (ULSI): more than 1 million transistors
  - There's no name after ULSI



Embedded processor PXA270 (200 thousands Tr)

Processor for PC Intel Atom (46 millions Tr)

Quiz

- How many transistors does latest LSI have?
  1. 100 millions transistors
  2. 300 millions transistors
  3. 1 billion transistors
  4. 3 billions transistors

Answer

- 4. “3 billion transistors”
  - Latest Intel Xeon has nearly 3 billions transistors
  - But many of them are used for cache SRAM

SRAM -> Chap. 5

Cache -> Chap. 11, 12

How to create such a LSI?

- Placing such a many transistors with hand designing is almost impossible
- Computer assistance is required
  - Computer Aided Design (CAD)
  - Design Automation (DA)
  - Electronic Design Automation (EDA)

In this lecture, I treat “the basic point of EDA”

Outlined flow of LSI design

- Define specification -> Chap. 11, 12
- Definition in hardware description language
  - Architectural design -> Chap. 4, 5, 6, 11, 12

Logic synthesis

- Circuit with basic logic gates
  - Logical design -> Chap. 2, 3, 4, 5, 7, 8

Place and route

- Mask pattern
  - Physical design -> Chap. 9, 10
- Manufacturing

Definition in Hardware Description Language (HDL)

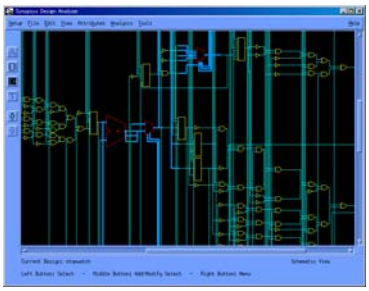
- e.g. Definition of chronograph with Verilog HDL

```
module stopwatch(reset,clock,switch,sec1_lap,sec2_lap,min_lap,lap);
  input reset,clock,switch,lap;
  output [3:0] sec1_lap;
  output [3:0] sec2_lap;
  output [3:0] min_lap;

  reg[3:0] sec1;     // 10sinn
  …
  always @ (posedge clock or negedge reset ) begin
    if(reset == 1'b0) begin
      sec1_lap <= 4'b0000;
      lap_state <= L1;
      …
endmodule
```

-> Chap. 4, 5, 6, 11, 12

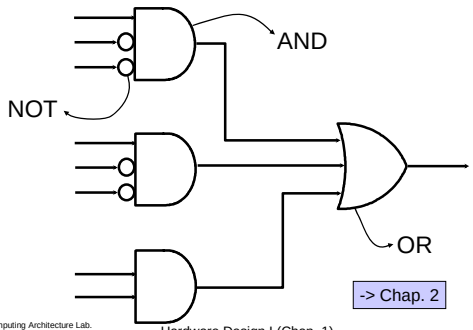
Circuit diagram after logic synthesis



- Represented as Register Transfer Level (RTL) notation
- The circuit is denoted with logic gate symbols and wire connection

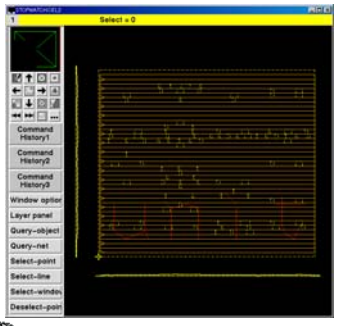
-> Chap. 2, 3, 4, 5, 7, 8

Outline of logic gate symbol



-> Chap. 2

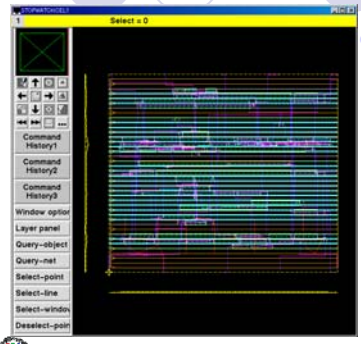
Place and route (1/2)



- Place logic cells into virtual silicon surface
- Each logic cell has designed in fix height and arbitrary diameter of unit width

-> Chap. 9, 10

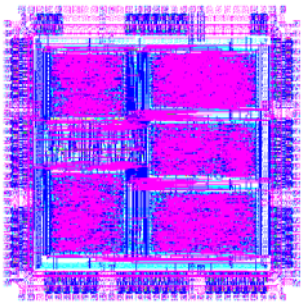
Place and route (2/2)



- Routing wires which connects logic cells

-> Chap. 9, 10

Layout of designed LSI



- Including pin layout for external connection

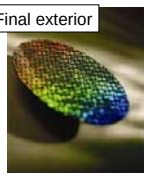
-> later Chap. 1

Outline of Chap. 1

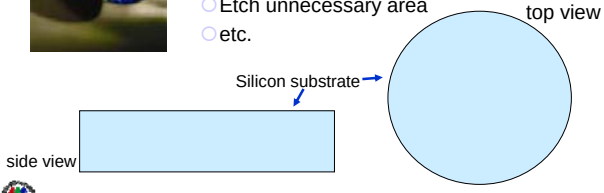
- Definition of digital system
- History of digital system
  - From vacuum bulb to field effective transistor (FET)
- The physical image of current device
  - Metal Oxide Semiconductor (MOS) FET
  - CMOS organization (CMOS NAND, CMOS NOR)
- Outlined flow of LSI design
- Outlined flow of semiconductor process

How to create CMOS

Final exterior

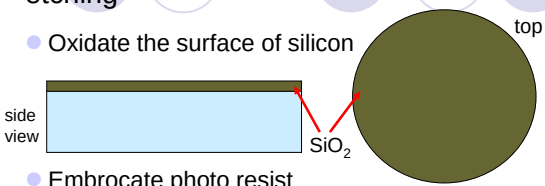


- By repeating following operation on silicon substrate
  - Injecting impurity
  - Deposit silicon or metal
  - Etch unnecessary area
  - etc.

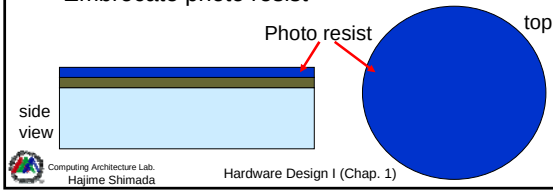


Creating SiO_2 coat and prepare for etching

- Oxidate the surface of silicon

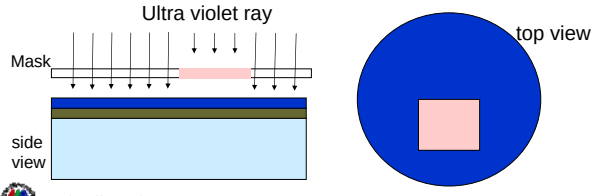


- Embrocate photo resist



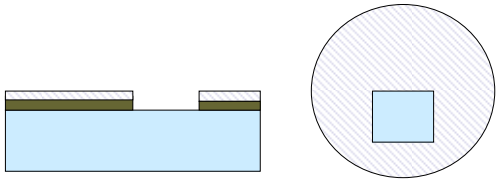
Exposure

- Expose ultra violet ray under mask
  - Requires 7-10 masks in total (2-3M yen per 1 mask)
  - Latest process uses 193nm ultra violet ray
- Exposed area becomes hard



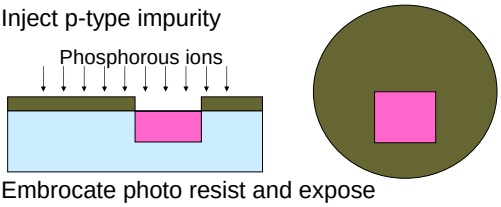
Etching

- Etches not harden photo resist and SiO_2
  - Dry etching: etches with gas
  - Wet etching: etches with drug solution
- After that, harden photo resist is removed



Creating p-well and ...

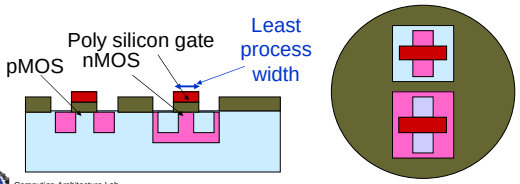
- Inject p-type impurity



- Embrocate photo resist and expose
- Inject n-type impurity
- Dope poly silicon
- ...

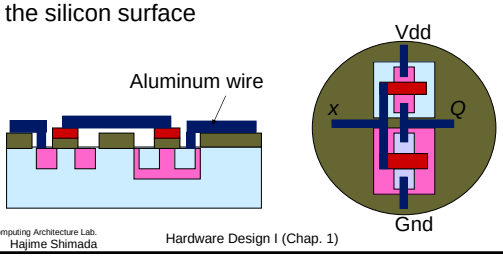
Create pMOS and nMOS

- After several processes...
- pMOS and nMOS transistor has created on the silicon surface



Create wire

- Create wire which conducts MOS transistors
  - Aluminum wire (traditional) or copper wire
- Finally we can create logic gates (or circuits) on the silicon surface



Advancement with shrinking

- Semiconductor advances with shrinking minimum process width
  - Enables much transistors into same size
  - Enables quick operation with reduces capacitance
- Industries shrinks it every 2 or 3 years
  - e.g. Intel's process technology: 90nm (2004), 65nm (2006), 45nm(2008), 32nm(2010)
- But physical bound is very close
  - Atom is countable even in current process technology
  - Do we have to move to the other devices?